(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
8 February 2001 (08.02.2001)

PCT

(10) International Publication Number
WO 01/09683 A1

(51) International Patent Classification[7]: G03F 7/09, 7/16

(21) International Application Number: PCT/US00/20383

(22) International Filing Date: 26 July 2000 (26.07.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/366,131 2 August 1999 (02.08.1999) US

(71) Applicant: INFINEON TECHNOLOGIES NORTH AMERICA CORP. [US/US]; 1730 North First Street, San Jose, CA 95112-6000 (US).

(72) Inventor: LEE, Gill, Yong; 41 Sherwood Heights, Wappingers Falls, NY 12590 (US).

(74) Agents: CODISPOTI, Joseph, S. et al.; Siemens Corporation - Intellectual Property Dept., 186 Wood Ave. South, Iselin, NJ 08830 (US).

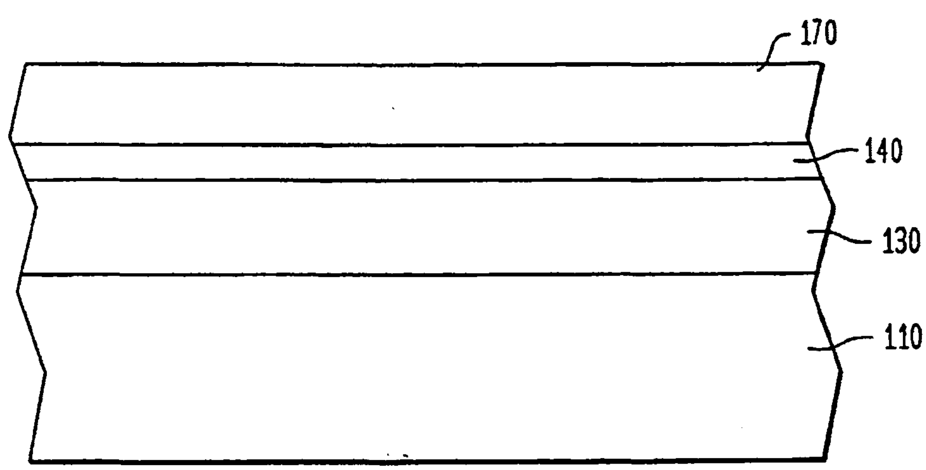
(81) Designated States *(national)*: CN, JP, KR.

(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published:
— *With international search report.*
— *Before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments.*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: REDUCTION OF RESIST POISONING



WO 01/09683 A1

(57) Abstract: A silicon-rich layer is provided beneath a resist to prevent resist poisoning by an underlying device layer.

REDUCTION OF RESIST POISONING

Field of the Invention

The invention relates generally to fabrication of devices such as integrated circuits. More particularly, the invention relates to the improving critical dimension control during patterning.

Background of the Invention

In the fabrication of devices such as integrated circuits (ICs), features are formed on a substrate. The features, for example, correspond to components such as transistors, capacitors, and resistors. These components are then interconnected to achieve the desired electrical function.

To form the devices, layers are repeatedly deposited on the substrate and selectively patterned. Lithographic techniques are used to pattern the device layer or layers. Such techniques typically use an exposure source to project a light image from a mask onto a photoresist (resist) layer formed on the surface of the substrate. The light illuminates the resist layer, exposing it with the desired pattern. Depending on whether a positive or negative tone resist is used, the exposed or unexposed portions of the resist layer are removed. The portions not protected by the resist are then, for example, etched to form the features in the substrate.

The imaging mechanism of photoresist is a photo-acid generator, which produces an acid to catalyze a chemical reaction in the resist when exposed to light. The chemical reaction changes the resist solubility, enabling

exposed or unexposed portions to be removed by a developer.

The dimensions of the features depend on the resolution capability of the lithographic systems. The minimum feature size (F) achieved by a given generation of lithographic systems is referred to as the lithographic groundrule (GR). Critical dimension (CD) is defined as the minimum feature size that must be controlled. This includes, for example, linewidths, spacings, and contact widths.

Due to the variations of light or reflectance into the resist layer, variations in CD occur. Controlling the variations in CD (CD control) becomes a critical issue, particularly with deep ultra-violet lithography (DUV). CD control is facilitated by the use of an antireflective coating (ARC) beneath the resist to reduce reflectance variations into the resist caused by underlying layers.

Inorganic ARCs, such as dielectric ARCs (DARCs), are attractive candidates for improving lithographic process window for DUV lithography. This is because inorganic ARCs possess desirable characteristics such as tunable properties, low defect levels, good conformality, high etch selectivity to resist, and small swing ratio.

However, the use of inorganic ARCs has been limited due to "resist poisoning." Resist poisoning refers to the contamination of the resist by, for example, amine radicals from the inorganic ARC, neutralizing the acid-generators which makes the contaminated portions of the resist insoluble by the developer. As a result, a foot in the resist profile is formed after development.

A conventional technique to prevent resist poisoning is to provide an oxide layer between the ARC and the resist layer. The oxide layer can be deposited on the ARC or formed by plasma treating the surface of the ARC. However, the oxide layer is ineffective in preventing resist poisoning with certain resist chemistry such as JSR TM 399 from JSR Microelectronics. In fact, the oxide layer seems to exacerbate the resist poisoning problem.

As evident from the above discussion, it is desirable to effectively reduce resist poisoning to improve the lithographic process window.

Description of the Drawings

Fig. 1 shows an illustrative embodiment of the invention; and

Figs. 2-3 show the resist profile with and without silicon treatment in accordance with the invention.

Summary of the Invention

The invention relates to reducing resist poisoning. In one embodiment, a cap layer is provided beneath the resist. In one embodiment, the cap layer comprises a silicon-rich layer. Preferably, the cap layer comprises an amorphous silicon layer. Alternatively, excess dangling bonds can be created on a device layer beneath the resist layer to reduce resist poisoning. By reducing resist poisoning, the lithographic process window can be improved.

Description of the Invention

The invention relates to the fabrication of devices, such as integrated circuits (ICs). In particular, the

invention relates to reducing resist poisoning in order to improve the lithographic process window. In accordance with the invention, resist poisoning is reduced by providing a cap layer comprising silicon beneath the resist.

Fig. 1 shows one embodiment of the present invention for reducing resist poisoning. As shown, a substrate 110 is provided. The substrate comprises, for example, a semiconductor substrate such as a silicon wafer. Other types of substrates such as those comprising gallium arsenide, germanium, silicon-on-insulator, or other semiconductor materials are also useful. Non-semiconductor substrates can also be used. The substrate can be at various stages of the process flow. For example, the substrate can be at the beginning of the process flow or partially processed to include features (not shown). The features are used to form, for example, integrated circuits (ICs) such as dynamic random access memories (DRAMs) or other types of ICs. The features can also be used to form electromechanical or mechanical devices. For purposes of discussion, the term "substrate" is used to refer to a substrate which can be at any stage in the process flow.

A device layer 130 is formed above the substrate. The device layer, in one embodiment, comprises an ARC layer. In one embodiment, the ARC layer comprises an inorganic ARC layer. The inorganic ARC layer comprises, for example, a DARC, such as silicon nitride (Si_xN_y), silicon oxynitride, (SiN_xO_y), hydrogenated silicon oxynitride, or other types of dielectric antireflective materials. In a preferred embodiment, the DARC comprises silicon oxynitride. Metallic ARCs or other inorganic

antireflective materials are also useful. The inorganic ARC layer is deposited using conventional techniques such as, for example, chemical vapor deposition (CVD).

In another embodiment, a multi-layer ARC stack utilizing absorption and destructive interference properties can be provided. Multi-lyaer ARC stacks are described in copending US patent application USSN ______________ (attorney docket number 98P 7982 US) titled "Improved CD Control", which is herein incorporated by reference for all purposes. An ARC layer comprising a graded refractive index is also useful. Graded refractive index ARC layers are described in copending US patent application USSN 09/276,026 (attorney docket number 98P 7982 US01) titled "Arc for improving CD control", and which is also herein incorporated by reference for all purposes.

Alternatively, the device layer 110 comprises a dielectric layer. Dielectric material such as silicon oxide, silicon nitride, or doped silicate glass such as boron-phosphorus-silicate glass, can be useful to serve as the device layer. Other types of dielectric materials are also useful. The dielectric layer can be formed using conventional techniques.

A thin cap layer 140 is formed over the device layer to reduce resist poisoning between the ARC and the subsequently formed resist. In accordance with one embodiment of the invention, the cap layer comprises silicon. Preferably, the cap layer comprises a thin amorphous silicon layer. The silicon comprising layer is sufficiently thin to avoid causing standing waves and interference in the resist. The cap layer, in one embodiment, is less than about 30Å thick, preferably less

than about 10Å thick, and more preferably less than about 3Å thick. The thickness of the cap layer can be optimized to produce the desired resist profile.

Alternatively, the cap layer comprises a mono-atomic layer that alters the surface morphology of the device layer. The mono-atomic layer, in one embodiment, comprises excess silicon dangling bonds on the surface of the device layer. In such a case, the cap layer comprises a silicon-rich layer. The composition of the cap layer depends on the underlying device layer. For example, the cap layer would comprise a silicon-rich oxide or silicon-rich oxynitride if the underlying device layer comprised a silicon oxide or an oxynitride layer.

The resist layer 170 comprises, for example, any conventional resist used in lithography. Such resist can either be positive or negative tone resist. In one embodiment, the resist comprises JSR TM 399. The resist is formed by conventional techniques. The thickness of the resist is, for example, sufficiently thick to serve as an etch mask for the ARC open process. Typically, the thickness of the resist layer is about 0.2 - 10 μm.

As described, the invention provides a silicon comprising cap layer underneath the resist to prevent resist poisoning. The high mismatch in the refractive indices of silicon and resist can cause standing waves or interference. However, since the cap layer is very thin (in some cases the thickness may not be measurable as in the case of a mono-atomic layer), the impact of standing waves or interference is reduced or minimized.

In one embodiment, the silicon cap layer is formed by chemical vapor deposition (CVD), such as low pressure CVD (LPCVD), plasma enhanced CVD (PECVD), high density

plasma CVD (CVD), electron cyclotron resonance (ECR) CVD. Other types of plasma processes such as PVD are also useful. A silicon precursor gas and a dilute gas or gas mixture are introduced into the chamber containing the substrate with the device layer. In one embodiment, a silicon precursor gas comprising SiH_4 is employed. Other types of silicon precursors such as TEOS and Si_2H_6 are also useful. Dilute gas can include, for example, helium (He), argon (Ar), or Neon (Ne). The gases react in the chamber, depositing the silicon cap layer on the device layer.

The process parameters of forming the cap layer are as follows:

RF plasma power	:	about 10 - 5,000 watts
chamber pressure	:	about 0.1 mTorr to 20 Torr
spacing between showerhead and wafer	:	about 10 - 5000 mils
silicon precursor flow rate (SiH_4)	:	about 0 - 100 sccm

The deposition process forms a thin cap layer comprising silicon on the surface of the device layer. Preferably, the cap layer comprises a thin amorphous silicon layer. The deposition process can also be used to alter the surface morphology of the device layer by creating excess silicon dangling bonds thereon. The silicon comprising cap layer, in one embodiment, is less than about 30Å thick, preferably less than about 10Å thick, and more preferably less than about 3Å thick. Typically, the process duration is about a range of 0.1 to 120 sec.

The process for forming the cap can be performed in the same process as the formation of the device layer (i.e., in-situ). For in-situ processes, the flow of

gases that are not needed for forming the cap layer into the chamber are turned off. The reactor power remains on and the flow of gases that are needed such as the silicon precursor and dilute (e.g., He) gases remain on or are turned on. For example, after forming a silicon oxynitride device layer by PECVD, the oxygen gas sources such as N_2O or O_2 are turned off while the RF plasma power, silicon precursor gas and dilute gas remain on to form the cap layer. The duration of the process is typically about 0.1 - 120 sec.

The gas flow rates, power settings, pressure, and other parameters can be gradually adjusted after the end of the formation of the device layer to the desired levels for forming the cap layer. A stabilization step can be performed prior to the commencement of the formation of the cap layer to stabilize gas flow rates. This is particularly useful when the gas flow regimes are different for the different processes.

Examples

Fig. 2 shows a SEM of a resist layer 270 formed over a silicon oxynitride ARC 230 without the silicon comprising cap layer as described. The resist was patterned to form openings 210. As seen from the SEM, the resist profile narrows at the bottom of the opening. This phenomenon is referred to as footing. Footing occurs as a result of resist poisoning from the oxynitride ARC. Footing is undesirable as it distorts the dimensions of the features that are to be formed.

Referring to Fig. 3, a silicon comprising cap layer 320 in accordance with one embodiment of the invention is provided between a resist layer 370 and a silicon

oxynitride ARC 370. Openings 310 were formed in the resist. The resist profile shows that the dimensions at the top and bottom of the openings are about the same, indicating that resist poisoning is avoided by the use of the silicon cap layer.

While the invention has been particularly shown and described with reference to various embodiments, it will be recognized by those skilled in the art that modifications and changes may be made to the present invention without departing from its scope. The scope of the invention should therefore be determined not with reference to the above description but with reference to the appended claims along with their full scope of equivalents.

What is claimed is:

1. In the fabrication of devices, a method for reducing resist poisoning comprising:

providing a substrate with a device layer;

depositing a cap layer comprising silicon on the device layer; and

depositing a resist layer over the cap layer.

2. The method of claim 1 wherein the device layer comprises an anti-reflective coating (ARC).

3. The method of claim 2 wherein the device layer comprises an inorganic ARC.

4. The method of claim 4 wherein the inorganic ARC comprises a dielectric ARC.

5. The method of claim 4 wherein the dielectric ARC is selected from a group consisting of

6. The method of claim 3 wherein the inorganic ARC is selected from a group consisting

7. The method of claim 1 wherein the device layer comprises a dielectric layer.

8. The method of claim 7 wherein the device layer is selected from a group consisting of

9. The method of claim 1, 2, 3, 4, 5, 6, 7, or 8 wherein the cap layer comprises a silicon-rich layer.

10. The method of claim 9 wherein the cap layer comprises an amorphous silicon layer.

11. The method of claim 10 wherein the cap layer is thin to avoid interference.

12. The method of claim 11 wherein the cap layer comprises a thickness of less than about 30Å

13. The method of claim 11 wherein the cap layer comprises a thickness of less than about 10Å

14. The method of claim 11 wherein the cap layer comprises a thickness of less than about 3Å

15. The method of claim 1, 2, 3, 4, 5, 6, 7, or 8 wherein forming the cap layer comprises forming excess dangling silicon bonds on the surface of the device layer.

16. The method of claim 15 wherein the excess dangling silicon bonds are formed by altering the surface morphology of the device layer.

17. The method of claim 15 wherein the cap layer is formed with in-situ process.

18. The method of claim 17 further comprises a stabilization step prior to forming the cap layer to stabilize flow of gases into a reaction chamber.

19. The method of claim 18 wherein forming the cap layer comprises leaving the reactor power and flow of silicon precursor and dilute gases while turning off flow of other gases after formation of the device layer.

20. The method of claim 17 wherein forming the cap layer comprises leaving the reactor power and flow of silicon precursor and dilute gases while turning off flow of other gases after formation of the device layer.

21. The method of claim 15 wherein forming the cap layer comprises:

introducing silicon precursor and dilute gases into a reaction chamber; and

causing a reaction to form the silicon cap layer.

22. The method of claim 1 wherein the cap layer is formed with in-situ process.

23. The method of claim 22 further comprises a stabilization step prior to forming the cap layer to stabilize flow of gases into a reaction chamber.

24. The method of claim 23 wherein forming the cap layer comprises leaving the reactor power and flow of silicon precursor and dilute gases while turning off flow of other gases after formation of the device layer.

25. The method of claim 22 wherein forming the cap layer comprises leaving the reactor power and flow of silicon precursor and dilute gases while turning off flow of other gases after formation of the device layer.

26. The method of claim 1 wherein forming the cap layer comprises:

introducing silicon precursor and dilute gases into a reaction chamber; and

causing a reaction to form the silicon cap layer.

27. The method of claim 9 wherein the cap layer is formed with in-situ process.

28. The method of claim 27 further comprises a stabilization step prior to forming the cap layer to stabilize flow of gases into a reaction chamber.

29. The method of claim 28 wherein forming the cap layer comprises leaving the reactor power and flow of silicon precursor and dilute gases while turning off flow of other gases after formation of the device layer.

30. The method of claim 27 wherein forming the cap layer c3omprises leaving the reactor power and flow of silicon precursor and dilute gases while turning off flow of other gases after formation of the device layer.

31. The method of claim 9 wherein forming the cap layer comprises:

introducing silicon precursor and dilute gases into a reaction chamber; and

causing a reaction to form the silicon cap layer.

32. The method of claim 10 wherein the cap layer is formed with in-situ process.

33. The method of claim 32 further comprises a stabilization step prior to forming the cap layer to stabilize flow of gases into a reaction chamber.

34. The method of claim 33 wherein forming the cap layer comprises leaving the reactor power and flow of silicon precursor and dilute gases while turning off flow of other gases after formation of the device layer.

35. The method of claim 32 wherein forming the cap layer comprises leaving the reactor power and flow of silicon precursor and dilute gases while turning off flow of other gases after formation of the device layer.

36. The method of claim 10 wherein forming the cap layer comprises:

introducing silicon precursor and dilute gases into a reaction chamber; and

causing a reaction to form the silicon cap layer.

37. The method of claim 11 wherein the cap layer is formed with in-situ process.

38. The method of claim 37 further comprises a stabilization step prior to forming the cap layer to stabilize flow of gases into a reaction chamber.

39. The method of claim 38 wherein forming the cap layer comprises leaving the reactor power and flow of silicon

precursor and dilute gases while turning off flow of other gases after formation of the device layer.

40. The method of claim 37 wherein forming the cap layer comprises leaving the reactor power and flow of silicon precursor and dilute gases while turning off flow of other gases after formation of the device layer.

41. The method of claim 11 wherein forming the cap layer comprises:

introducing silicon precursor and dilute gases into a reaction chamber; and

causing a reaction to form the silicon cap layer.

42. The method of claim 1 wherein the device comprises an integrated circuit.

43. The method of claim 1 wherein the device comprises memory integrated circuit.

FIG. 1

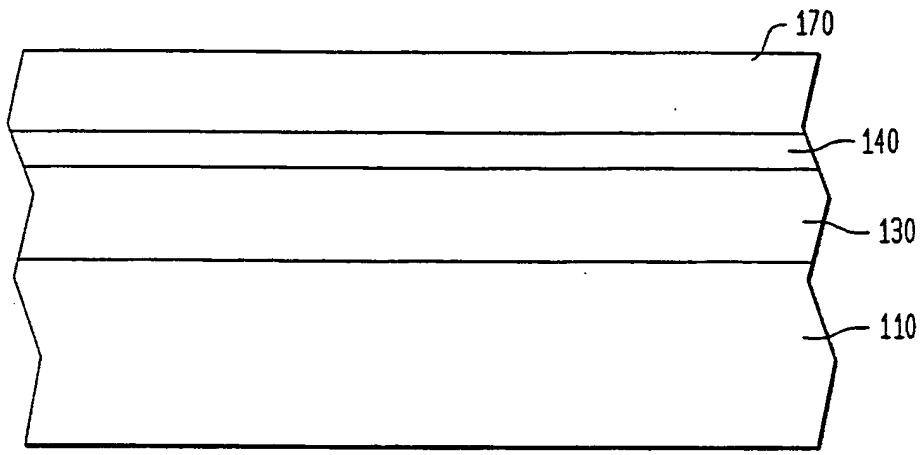


FIG. 2

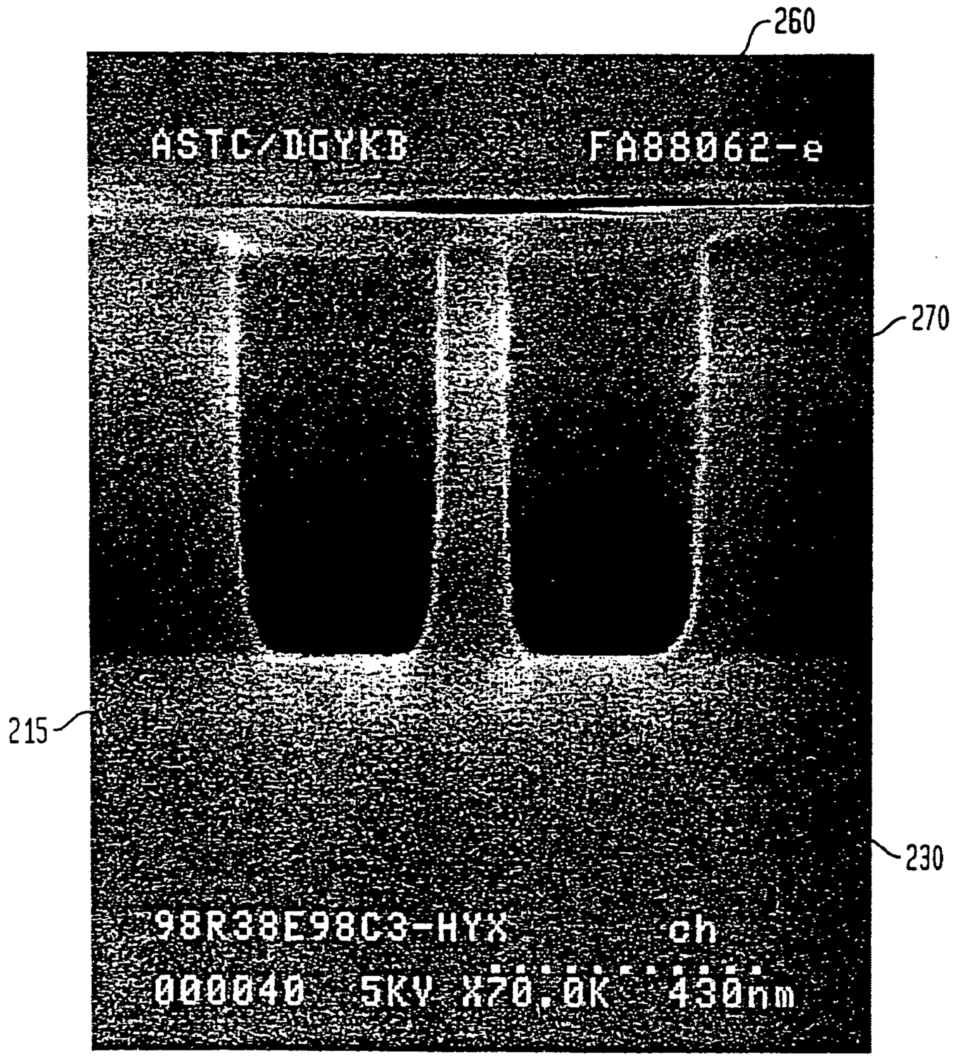
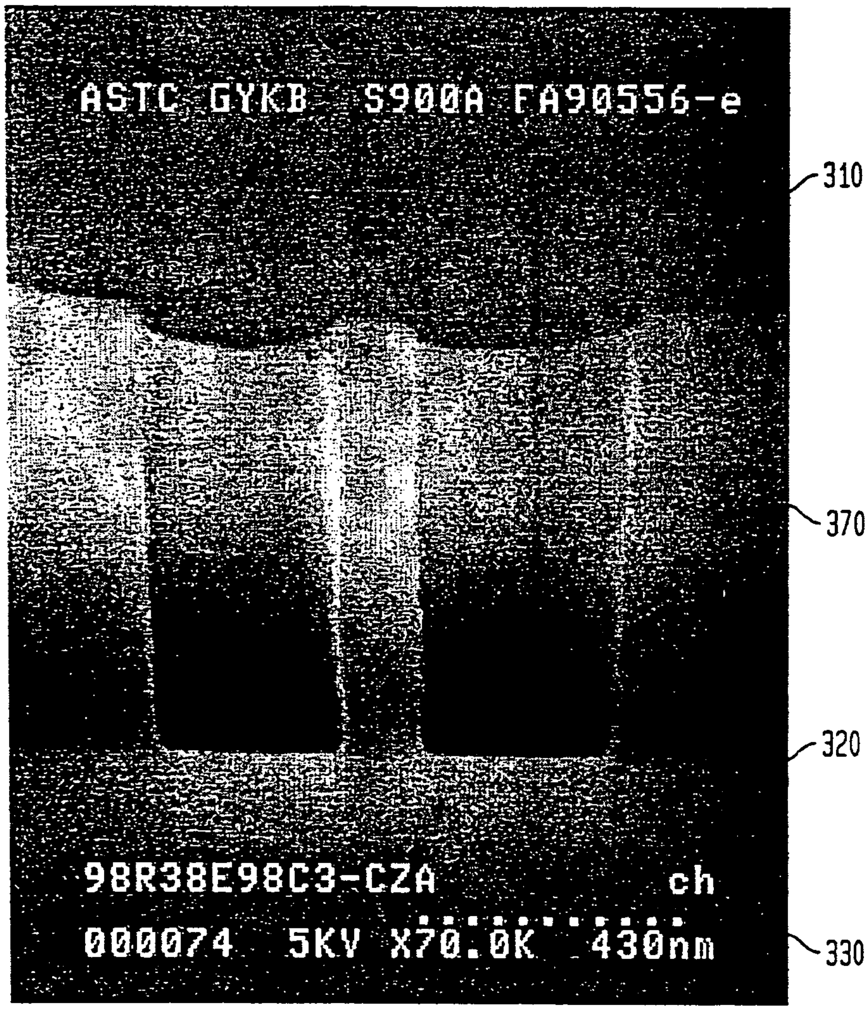

260
270
215
230
ASTC/DGYKB
FA88062-e
98R38E98C3-HYX
ch
000040 5KV X70.0K 430nm

FIG. 3


ASTC GYKB S900A FA90556-e
98R38E98C3-CZA ch
000074 5KV X70.0K 430nm
310
370
320
330

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 00/20383

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G03F7/09 G03F7/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, INSPEC, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	STEPHEN A ET AL: "Antireflective coating strategies for 193 nm lithography", PROCEEDINGS OF THE SPIE,SPIE, BELLINGHAM, VA,US, VOL. 3678, PT.1-2, PAGE(S) 1315-1322 XP002150384 the whole document ---	1-9, 22-35, 42,43
X	BASSOUS E ET AL: "TRIPLE LAYER SYSTEM FOR HIGH RESOLUTION MICROLITHOGRAPHY" IBM TECHNICAL DISCLOSURE BULLETIN,US,IBM CORP. NEW YORK, vol. 25, no. 11B, April 1983 (1983-04), pages 5916-5917, XP000807495 ISSN: 0018-8689 the whole document ---	1,9,10, 26,27, 31,32, 36,37, 42,43

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 November 2000	14.12.2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Haenisch, U

2

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 00/20383

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 840 361 A (APPLIED MATERIALS INC) 6 May 1998 (1998-05-06) the whole document	1-9, 22-35, 42,43
X	EP 0 757 290 A (MATSUSHITA ELECTRIC IND CO LTD ;SHINETSU CHEMICAL CO (JP)) 5 February 1997 (1997-02-05)	1
A	the whole document	15,16
X	GB 2 145 243 A (GEN ELECTRIC) 20 March 1985 (1985-03-20) the whole document	1,9-11
A	US 5 783 365 A (TSUJITA KOUICHIROU) 21 July 1998 (1998-07-21) figure 3	
A	MORI S ET AL: "INVESTIGATION OF SUBSTRATE-EFFECT IN CHEMICALLY AMPLIFIED RESIST" , PROCEEDINGS OF THE SPIE XP000956033 figure 2	

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 00/20383

Box I Observations wher certain claims were found unsearchable (Continuati n of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 5 6 8 15-25
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:
see FURTHER INFORMATION sheet PCT/ISA/210

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional s arch fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

Continuation of Box I.2

Claims Nos.: 5 6 8 15-25

Claims 5 6 8 do not specifiy the groups from which the ARC layer and the device layer are chosen from respectively.

Claims 15-22: the concept of a "capping layer" is not consistent with "forming excess dangling silicon bonds on the surface of the device layer":

- Either the silicon characterised by the dangling bonds must be part of the capping layer, but then the bonds are not "on the surface of the device layer";
- or the silicon originates from elements already part of the device layer, in which case it cannot be described as "cap layer on the device layer", as specified in claim 1.

Neither the claims nor the description contain sufficient information to allow a clear interpretation of these features.

The applicant's attention is drawn to the fact that claims, or parts of claims, relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 00/20383

Patent document cited in search report		Publication date	Patent family member(s)			Publication date
EP 0840361	A	06-05-1998	JP	10189441	A	21-07-1998
EP 0757290	A	05-02-1997	JP	9102458	A	15-04-1997
GB 2145243	A	20-03-1985	DE	3428565	A	07-03-1985
			JP	60074529	A	26-04-1985
US 5783365	A	21-07-1998	JP	8172039	A	02-07-1996
			KR	169160	B	01-02-1999